WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory comprising:

a memory cell array in which one block for writing/erasing a page unit comprises pages; and

a control circuit which manages, for each page, information associated with the number of data write/erase times with respect to each of the pages.

2. The nonvolatile semiconductor memory according to claim 1, wherein the nonvolatile semiconductor memory has a page erase function.

3. The nonvolatile semiconductor memory according to claim 1, wherein the control circuit is mounted in the nonvolatile semiconductor memory in a mixed manner.

4. The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in a redundancy area of the memory cell array in the nonvolatile semiconductor memory.

5. The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in a special memory cell area different from the memory cell array in the nonvolatile semiconductor memory.

6. The nonvolatile semiconductor memory according to claim 1, wherein the information is stored in another nonvolatile semiconductor memory different from the nonvolatile semiconductor memory.

7. The nonvolatile semiconductor memory according to claim 1, wherein the control circuit reads the

information with respect to all the pages every time data is written/erased.

8. The nonvolatile semiconductor memory according to claim 7, wherein the control circuit renews the information with respect to the page which is an object of the data write/erase every time data is written/erased.

9. The nonvolatile semiconductor memory according to claim 8, wherein the data write/erase is performed by reading the information, subsequently erasing the data of the page which is the object of data write/erase, and writing renewed data in the page which is the object of data write/erase.

10. The nonvolatile semiconductor memory according to claim 8, wherein the control circuit determines whether or not to perform refresh for returning states of memory cells of all the pages in the block or the page which is the object of data write/erase to initial states based on the information on all the pages every time the data is written/erased.

11. The nonvolatile semiconductor memory according to claim 10, wherein the renew of the information is performed by setting the information on the page which is the object of data write/erase to the number of data write/erase times of the page which is the object of data write/erase.

12. The nonvolatile semiconductor memory according

to claim 11, wherein the refresh is executed, when a total value of the number of data write/erase times reaches an allowable value with respect to all the pages.

13. The nonvolatile semiconductor memory according to claim 12, wherein the information is initialized by the refresh.

14. The nonvolatile semiconductor memory according to claim 10, wherein the renew of the information is performed by setting the information on the page which is the object of data write/erase to a total value of the number of data write/erase times in the block.

15. The nonvolatile semiconductor memory according to claim 14, wherein the refresh is executed, when a maximum value of the number of data write/erase times reaches an allowable value with respect to all the pages.

16. The nonvolatile semiconductor memory according to claim 15, wherein the information is initialized by the refresh.

17. The nonvolatile semiconductor memory according to claim 14, wherein the refresh is executed, when a value obtained by subtracting a minimum value from a maximum value of the number of data write/erase times reaches an allowable value with respect to all the pages.

18. The nonvolatile semiconductor memory according

to claim 17, wherein the information is initialized by the refresh.

19. The nonvolatile semiconductor memory according to claim 17, wherein the information on the page which is an object of the refresh is renewed by the refresh.

20. The nonvolatile semiconductor memory according to claim 10, wherein the data write/erase is performed as a part of the refresh.

21. The nonvolatile semiconductor memory according to claim 1, wherein the nonvolatile semiconductor memory is a NAND-type flash memory.

22. A memory system comprising:

a memory cell array in which one block for performing a data write/erase operation by a page unit comprises pages; and

a controller which manages information associated with the number of data write/erase times with respect to each of the pages for each page.

23. The memory system according to claim 22, wherein the memory system constitutes a memory card.

24. The memory system according to claim 22, wherein the memory system comprises an electronic apparatus comprising: a memory card including the nonvolatile semiconductor memory; and the controller.

25. A nonvolatile semiconductor memory comprising:

a memory cell array in which one block for performing a data write/erase operation by an area unit

comprises areas; and

a control circuit which manages, for each area, information associated with the number of data write/erase times with respect to each of the areas.

26. The nonvolatile semiconductor memory according to claim 25, wherein each of the areas includes pages.

27. A memory system comprising:

a memory cell array in which one block for performing a data write/erase operation by an area unit comprises areas; and

a controller which manages information associated with the number of data write/erase times with respect to each of the areas for each area.

28. The memory system according to claim 27, wherein each of the areas includes pages.

29. The memory system according to claim 27, wherein the memory system constitutes a memory card.

30. The memory system according to claim 27, wherein the memory system comprises an electronic apparatus comprising: a memory card including the nonvolatile semiconductor memory; and the controller.

31. A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second memory areas in which one block comprises pages; and

a control circuit which manages, for each page, information associated with the number of data write/erase times with respect to each of the pages,

wherein the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

32. A memory system comprising:

a memory cell array comprising first and second memory areas in which one block comprises pages; and

a controller which manages information associated with the number of data write/erase times with respect to each of the pages for each page,

wherein the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

33. A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second memory areas in which one block comprises areas; and

a control circuit which manages, for each area, information associated with the number of data write/erase times with respect to each of the areas,

wherein the area comprises pages, and the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

34. A memory system comprising:

a memory cell array comprising first and second memory areas in which one block comprises areas; and

a controller which manages information associated with the number of data write/erase times with respect

to each of the areas for each area,

wherein the area comprises pages, and the information is alternately stored in one of the first and second memory areas every time the data is written/erased.

35. A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second blocks comprising pages; and

a control circuit which manages, for each page, information associated with the number of data write/erase times with respect to each of the pages,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

36. A memory system comprising:

a memory cell array comprising first and second blocks comprising pages; and

a controller which manages information associated with the number of data write/erase times with respect to each of the pages for each page,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

37. A nonvolatile semiconductor memory comprising:

a memory cell array comprising first and second blocks comprising areas; and

a control circuit which manages, for each area,

information associated with the number of data write/erase times with respect to each of the areas,

wherein the area comprises pages, and the information is alternately stored in one of the first and second blocks every time the data is written/erased.

38. A memory system comprising:

a memory cell array comprising first and second blocks comprising areas; and

a controller which manages information associated with the number of data write/erase times with respect to each of the areas for each area,

wherein the area comprises pages, and the information is alternately stored in one of the first and second blocks every time the data is written/erased.

39. A nonvolatile semiconductor memory comprising:

a memory cell array comprising a first block comprising pages; and

a control circuit which manages, for each page, information associated with the number of data write/erase times with respect to each of the pages,

wherein the information is alternately stored in one of the first block and a second block in another nonvolatile semiconductor memory including the same constitution as that of the nonvolatile semiconductor memory every time the data is written/erased.

40. A memory system comprising:

a first nonvolatile semiconductor memory which comprises a first block comprising pages and which writes/erases data by a page unit;

a second nonvolatile semiconductor memory which comprises a second block comprising pages and which writes/erases the data by the page unit; and

a controller which manages information associated with the number of data write/erase times with respect to each of the pages for each page,

wherein the information is alternately stored in one of the first and second blocks every time the data is written/erased.

41. A memory system comprising:

a nonvolatile semiconductor memory in which a block comprises pages and in which each of the pages comprises memory cells disposed in a row direction and which has a function of selecting block erase to be performed by a unit of the block and page erase to be performed by a unit of the page; and

a control circuit which issues a command for executing the page erase to the nonvolatile semiconductor memory.

42. The memory system according to claim 41, wherein the page erase is a function of erasing unnecessary data in at least one page in data stored in the block.

43. The memory system according to claim 41, wherein the control circuit manages information associated with the number of data write/erase times with respect to each of the pages for each page.

44. The memory system according to claim 43, wherein the control circuit manages whether or not a value obtained by subtracting a minimum value from a maximum value reaches an allowable value in the information on all the pages.

45. The memory system according to claim 41, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

46. A control method of a nonvolatile semiconductor memory in which a block comprises pages and in which each of the pages comprises memory cells arranged in a row direction and which has a function of selecting block erase to be performed by a unit of the block and page erase to be performed by a unit of the page, the method comprising:

erasing unnecessary data in at least one page in data stored in the block by the page erase.

47. The control method according to claim 46, wherein the control circuit manages information associated with the number of data write/erase times

with respect to each of the pages for each page.

48. The control method according to claim 46, wherein the control circuit manages whether or not a value obtained by subtracting a minimum value from a maximum value reaches an allowable value in the information on all the pages.

49. The control method according to claim 46, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

50. A nonvolatile semiconductor memory comprising:

a memory cell array in which a block comprises pages and in which each of the pages comprises memory cells arranged in a row direction;

a function of selecting block erase to be performed by a unit of the block and page erase to be performed by a unit of the page; and

a function of managing information associated with the number of data write/erase times with respect to each of the pages for each page.

51. The nonvolatile semiconductor memory according to claim 50, wherein the page erase is a function of erasing unnecessary data in at least one page in data stored in the block.

52. The nonvolatile semiconductor memory according

to claim 50, wherein the nonvolatile semiconductor memory comprises a cell row comprising series-connected memory cells, one end of the cell row is connected to a source line, and the other end of the cell row is connected to a bit line.

53. A memory system comprising: the nonvolatile semiconductor memory according to claim 50.